

**B.TECH.****THEORY EXAMINATION (SEM–VI) 2016-17  
ADVANCE DIGITAL DESIGN USING VERILOG***Time : 3 Hours**Max. Marks : 100**Note : Be precise in your answer. In case of numerical problem assume data wherever not provided.***SECTION – A****1. Explain the following:****10 x 2 = 20**

- (a) What are the advantages of HDLs?
- (b) Differentiate between the unary and ternary operator.
- (c) Differentiate between \$monitor and \$display.
- (d) What are the differences between assignments in always and initial constructs?
- (e) Given the following Verilog code, what value of “a” is displayed?  

```
always @ (clk) begin
a=0;
a<=1;
$display(a);
```
- (f) What is the difference between the equality operator symbols == and ===?
- (g) What are the differences between a task and a function?
- (h) What are the modeling memory components in verilog?
- (i) Differentiate between Feedback model & Implicit model.
- (j) What are the benefits of assertion verifications.

**SECTION – B****2. Attempt any five of the following questions:****5 x 10 = 50**

- (a) (i) What is verilog HDL? What are the major capabilities of verilog HDL?  
(ii) Explain the components of a verilog module with block diagram.
- (b) (i) What are the different data types in verilog HDL ? Explain briefly.  
(ii) Illustrate the differences between a scalar and a vector. Explain with the help of suitable example.
- (c) (i) Explain NOR gate primitive with verilog module.  
(ii) Write verilog HDL source code for a gate level description of 4to 1 multiplexer circuit. Draw the relevant logic diagram.
- (d) (i) Explain inertial and intra-assignment delays in verilog with suitable example.  
(ii) Describe a module 2 to 4 demultiplexer through procedural continuous assignments.
- (e) (i) Define blocking and non blocking assignments using examples.  
(ii) Write a module using the behaviour modelling style to describe the behaviour of aJ-K flip-flop using an always statement.
- (f) (i) Describe a module for an NMOS inverter with an active pull up level using switch level primitives.  
(ii) Describe a module for NAND gate using MOS switches & write its test bench .
- (g) (i) Explain the use of path delay assignments in verilog with the help of suitable example.  
(ii) Write a verilog module for half adder using file based task & function and write also its test bench.
- (h) (i) What is a function of fork-join construct ? Design a verilog module for D flip flop using this construct.  
(ii) Write and explain the Verilog module for edge trigger flip-flop.

### SECTION – C

**Attempt any two of the following questions:**

**2 x 15 = 30**

- 3** (i) Design a FSM to detect 1001 sequence using Mealy machine.  
(ii) Design a module for a 2-bit priority encoder using 'casez' statement and test bench for the same.
- 4** (i) What do you understand from BDD and OBDD ? Explain with example.  
(ii) Design a verilog module for Gray-code counter.
- 5** (i) Design a full adder using gate level modelling in verilog HDL.  
(ii) Design a 16:1 Multiplexer using 8:1 MUX in verilog HDL.