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BTECH
(SEM III) THEORY EXAMINATION 2020-21
DIGITAL SYSTEM DESIGN

Time: 3 Hours

Total Marks: 100

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief.

Q no.	Question	Marks	CO
a.	Construct full adder using logic gates.	2	
b.	What is the concept of “setup” and “Hold” time?	2	
c.	What is difference between flip flop and latches?	2	
d.	What is difference between “Ripple Carry Adder” and Carry Look-ahead Generator?	2	
e.	How many flip flops are needed to implement a 32 bit register?	2	
f.	What is barrel shifter?	2	
g.	Which gates are called universal gates and why?	2	
h.	Differentiate between combinational logic circuit and sequential circuits?	2	
i.	Convert binary code(00011011) to gray code.	2	
j.	Implement a 4:1 multiplexer using 2:1 multiplexer.	2	

SECTION B

2. Attempt any three of the following:

Q no.	Question	Marks	CO
a.	Convert the following i. Hexadecimal equivalent of the decimal number 256 ii. Decimal equivalent of (123) ₉ iii. 378.93 ₁₀ to octal iv. Convert A3BH and 2F3H into binary.	10	
b.	Simplify using k-map to obtain a minimum POS expression: $(A'+B'+C+D)(A+B'+C+D)(A+B+C'+D'')(A'+B+C'+D')(A+B+C'+D)$	10	
c.	State and Prove Demorgan's theorem.	10	
d.	For the clocked JK flip-flop write the state table, draw the state diagram and the state equation.	10	
e.	Design a BCD adder using two 4 bit addresses.	10	

SECTION C

3. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	With the help of a neat diagram, explain the working of a two-input TTL NAND gate	10	
b.	With the help of a neat diagram, explain the working of any two I. a CMOS inverter, II. a two input CMOS NAND gate III. a two input CMOS NOR gate	10	



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4. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Define the following terms I. threshold voltage II. II. propagation delay III. III. power dissipation IV. IV. fan-in V. V. fan-out	10	
b.	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10	

5. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Explain the operation of FLASH ADC.	10	
b.	Explain the operation of successive approximation ADC. Discuss its merits and demerits.	10	

6. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Design a sequential circuit with two flip-flops, A & B and one input x. when x=0, the state of the circuit remains the same when x=1 the circuit passes through the state transitions from 00 to 01 to 11 to 10 back to 00 & repeat.	10	
b.	Explain 4bit Johnson counter with circuit diagram and waveforms.	10	

7. Attempt any one part of the following:

Q no.	Question	Marks	CO
a.	Design and implement a synchronous 3-bit up/down counter using JK flip-flops.	10	
b.	With a neat diagram explain the operation of R-2R DAC.	10	