

Paper Id: 130322Roll No:

B. TECH.
(SEM-III) THEORY EXAMINATION 2019-20
DIGITAL SYSTEM DESIGN

Time: 3 Hours

Total Marks: 100

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

2 x 10 = 20

Qno.	Question	Marks	CO
a.	The solution to the quadratic equation $k^2 - 11k + 22 = 0$ are $x = 3$ and $x = 6$. What is the base of the number system?	2	1
b.	Simplify the expression $F(A, B, C, D) = ACD + \bar{A}B + \bar{D}$ by K-Map.	2	1
c.	Construct half subtractor using logic gates.	2	2
d.	Implement a 4:1 multiplexer using 2:1 multiplexer.	2	2
e.	What do you mean by race around condition in JK Flip Flop?	2	3
f.	Distinguish between Latch and Flip Flop.	2	3
g.	What is logic family? Give the classification of logic families in brief.	2	4
h.	Describe figure of merit & noise immunity of TTL & CMOS ICs.	2	4
i.	What are the advantages and disadvantages of flash type ADC?	2	5
j.	The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0Volts, what is the output for an input of 101101111?	2	5

SECTION B

2. Attempt any *three* of the following:

3 x 10 = 30

Qno.	Question	Marks	CO
a.	Design an excess-3 to BCD code converter.	10	1
b.	Implement a full adder by using 8:1 multiplexer.	10	2
c.	Design a sequential circuit with two Flip Flops, A & B and one input x. When $x=0$, the State of the circuit remains the same when $x=1$ the circuit passes through the state transitions from 00 to 01 to 11 to 10 back to 00 & repeat.	10	3
d.	Compare TTL and CMOS logic families and also draw CMOS NOR gate.	10	4
e.	Explain the operation of successive approximation ADC. Discuss its merits and demerits.	10	5

SECTION C

3. Attempt any *one* part of the following:

1 x 10 = 10

Qno.	Question	Marks	CO
a.	Minimize the logic function using Quine-McCluskey Method $F(A, B, C, D, E) = \sum m(8, 9, 10, 11, 13, 15, 16, 18, 21, 24, 25, 26, 27, 30, 31)$	10	1
b.	Simplify the logic expression using K-Map $F(A, B, C, D, E, F) = \sum m(0, 5, 7, 8, 9, 12, 13, 23, 24, 25, 28, 29, 37, 40, 42, 44, 46, 55, 56, 57, 60, 61)$	10	1

4. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Design a 4-bit parallel binary Adder/Subtractor circuit.	10	2
b.	Design a 4-bit comparator circuit using logic gates.	10	2

5. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10	3
b.	For the given state diagram design the circuit using T flip flop	10	3

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graph TD
    000((000)) -- "0/0" --> 010((010))
    000 -- "1/1" --> 001((001))
    010 -- "0/0" --> 010
    010 -- "1/1" --> 110((110))
    110 -- "0/0" --> 110
    110 -- "1/0" --> 100((100))
    001 -- "0/0" --> 001
    001 -- "1/1" --> 100
    100 -- "0/0" --> 100
    100 -- "1/1" --> 001
    
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6. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Draw three input standard TTL NAND gate circuit and explain its operation.	10	4
b.	Implement the following function using PLA $F_1 = \sum m(0,3,4,7)$ $F_2 = \sum m(1,2,5,7)$	10	4

7. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	With a neat diagram explain the operation of R-2R DAC.	10	5
b.	With a neat sketch explain the operation of Flash ADC.	10	5