

**B TECH**  
**(SEM-III) THEORY EXAMINATION, 2018-19**  
**DIGITAL LOGIC DESIGN**

Time: 3 Hours

Max. Marks: 70

Note: Be precise in your answer. In case of numerical problem assume data wherever not provided.

**SECTION-A**

**1. Attempt all of the following questions: (2×7=14)**

- (a) What is modulus of a counter?
- (b) How many flip flops are required to design Mod-5 Ring counter and Mod-5 Johnson counter?
- (c) Determine the value of base x, if :  $(193)_x = (623)_8$
- (d) Write the advantage of Gray code over the straight binary number sequence.
- (e) What do you mean by fan-out and fan-in?
- (f) Define cyclic codes.
- (g) What is race around condition?

**SECTION-B**

**2. Attempt any three of the following questions: (7×3 = 21)**

- (a) Minimize the following Boolean function using K- map.  
 $F(A, B, C, D) = \sum (3, 4, 5, 7, 9, 13, 14, 15)$
- (b) Minimize the following using Quine- McCluskey method.  
 $F(A, B, C, D) = \sum (0, 1, 9, 15, 24, 29, 30) + \sum d (8, 11, 31)$
- (c) Write short notes on priority encoder.
- (d) Implement the following Boolean function :  
 $F(A, B, C, D) = \sum (0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$  using  
 (i) 4:1 MUX  
 (ii) 2:1 MUX
- (e) Design Binary code to Gray code converter.

**SECTION - C**

**3. Attempt any one of the following questions: (7×1 = 7)**

- (a) (i) Draw a BCD adder circuit and explain its working.  
 (ii) Convert the SR Flip Flop to JK Flip Flop.
- (b) What do you mean by shift register? What is the need of shift register? Draw and explain bidirectional shift register.

**4. Attempt any one of following questions: (7×1 = 7)**

- (a) (i) Design a modulo-4 UP/DOWN counter using JK flip flop.  
 (ii) Design a ripple decade counter using JK flip flop.
- (b) (i) What is critical race and non- critical race? How can they be avoided?  
 (ii) Describe the hazards in digital circuits. How are these removed? Design a hazards free circuit of the following Boolean function:  
 $F(A, B, C) = \sum m (1, 2, 3, 5)$

**5. Attempt any one of following questions: (7×1 = 7)**

- (a) (i) Describe the circuit and performance of CMOS inverter and state the characteristics of CMOS.  
 (ii) Differentiate between PLA and PAL. Realize the full adder circuit using PAL.
- (b) (i) Discuss the concept of field programmable gate array (FPGA). Discuss the various structures of FPGA.  
 (ii) Tabulate the truth table for 8×4 ROM that implements the Boolean function:  
 $A(x, y, z) = \sum (1, 2, 4, 6)$   
 $B(x, y, z) = \sum (0, 1, 6, 7)$   
 $C(x, y, z) = \sum (2, 6)$   
 $D(x, y, z) = \sum (1, 2, 3, 5, 7)$

6. Attempt any one of following questions:

(7×1= 7)

- (a) An asynchronous sequential logic circuit is described by the following excitation and output function

$$y = X_1X_2 + (X_1 + X_2) Y$$

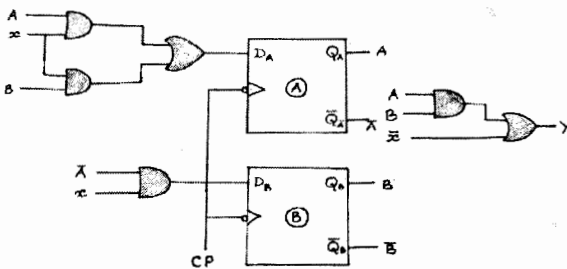
$$Z = y$$

- (i) Draw the logic diagram of the circuit.
  - (ii) Derive the transition table and output map
  - (iii) Describe the behavior of the circuit.
- (b) (i) The code 101101010 is received, correct any errors. There are four parity bits and odd parity is used.  
 (ii) Draw a full subtractor circuit using NAND gate.

7. Attempt any one of following questions:

(7×1= 7)

- (a) Drive the state table and state diagram for the Sequential circuit shown in fig.



- (b) Draw the reduced state table and reduced state diagram for the state table given below:

